

















Cäribou: A Versatile Data Acquisition System for Silicon Pixel Detector Characterization

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What is it and why is it?



A particular solution to a particular need

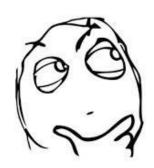
Most silicon pixel detectors share the same power, control and readout concepts (voltage/current supply, high speed data, communication protocols)

Pixel Interface FPGA Software device electronics processing



A particular solution to a particular need

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Every new prototype drives the development of a new DAQ system or modification of an exisiting one (time consuming, not very efficient)

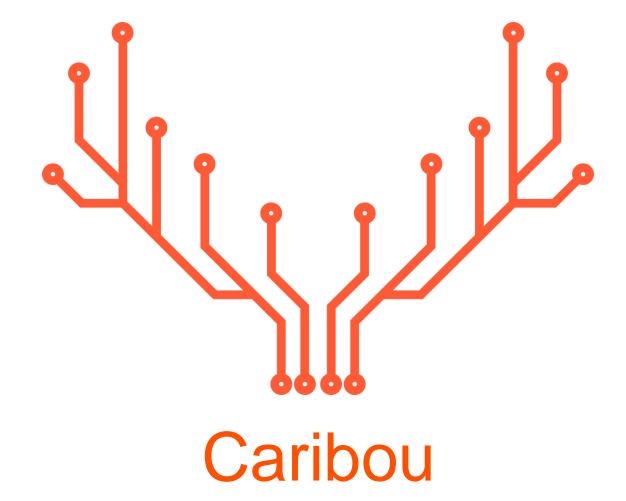
Why not a common versatile DAQ system?

(Common hardware, firmware and software suit, keeping the focus of users on detector integration)





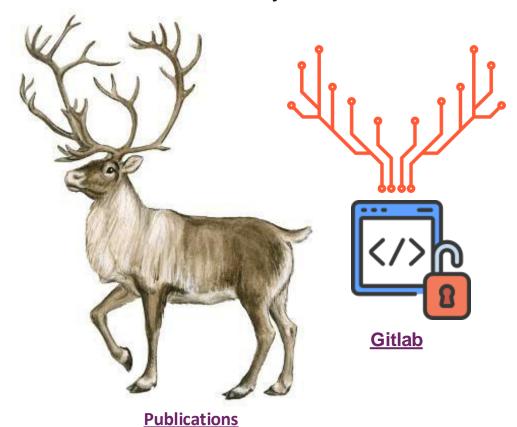
A particular solution to a particular need





Collaborating towards the open

Open source hardware, firmware and software for laboratory and beam tests

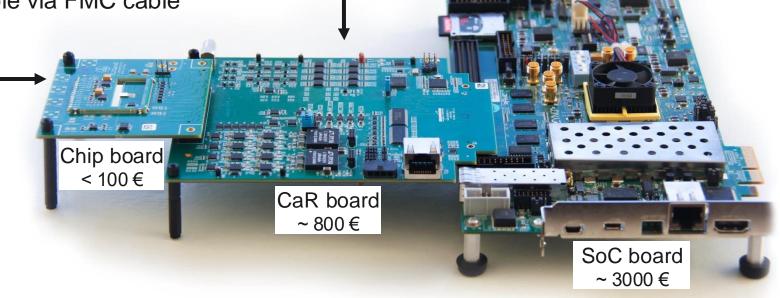


Developped by a collective effort of hardware, firmware and software developers



A simple system architecture

- System-on-Chip (SoC) board
 - ie: Xilinx ZC706 evaluation board
 - Embedded CPU runs DAQ and control software
 - FPGA runs custom firmware for detector control and readout
- Control and Readout (CaR) interface board
 - Physical interface from SoC to detector
 - CaR SoC connection extendable via FMC cable
- Detector (chip) carrier board
 - Custom low-cost PCB
 - Designed by users

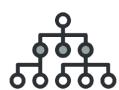


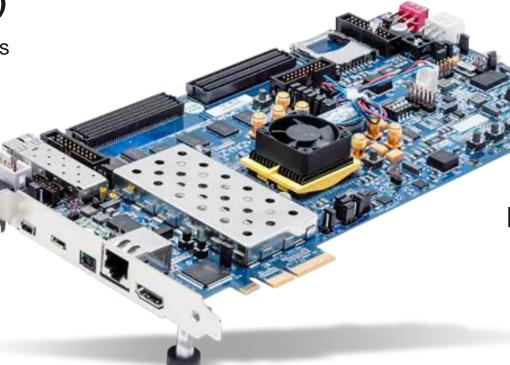


A commercial System-on-Chip board

Processing System (PS)

2 x ARM Cortex-A9 MPCore CPUs Petalinux image Network/ssh control interface Caribou software





Xilinx **ZC706** evaluation board

Programmable Logic (PL)

Kintex-7 FPGA
AXI control interface
Caribou firmware



A multifeature CaR board

Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 − 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, $0 - 1 \text{ V}$
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector

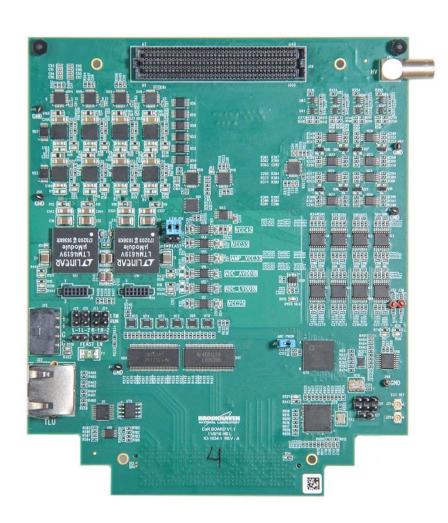
Resources for various target applications





More than 50 CaR boards to 14 institutes

Production and distribution coordinated by WP-1.4



A custom detector chip board

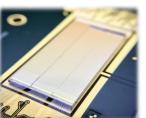
- Detector-specific
 - Physical hardware hosting the detector
 - Only provide passives and detector-specific components
- Multiple detectors already integrated and tested:

H2M



RD50-MPW2

M ATLASpix

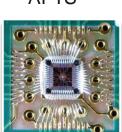


RD50-MPW3



CLICpix2

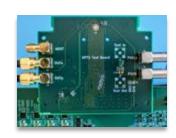
APTS



CLICTD



DPTS



FASTPIX



dSiPM



H35Demo/FEI4



MLR1



RD50-MPW1



CoRDIA



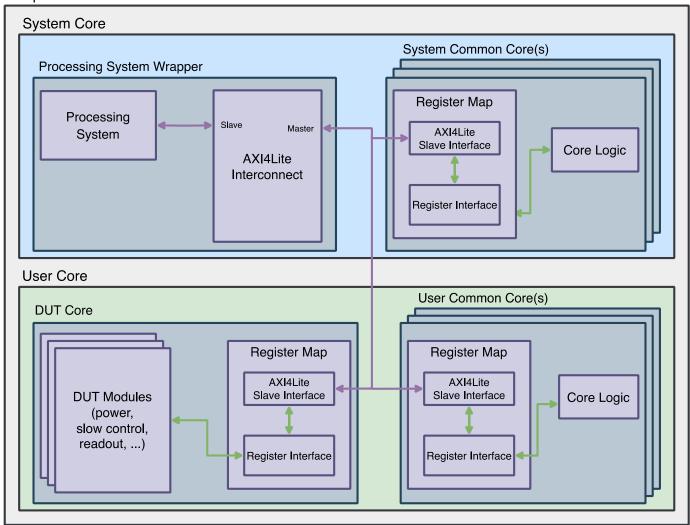


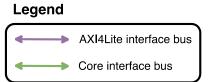
What else?



Caribou Boreal firmware







Unified, modular and configurable

Streamlined CI/CD workflow

Linting, simulation, building

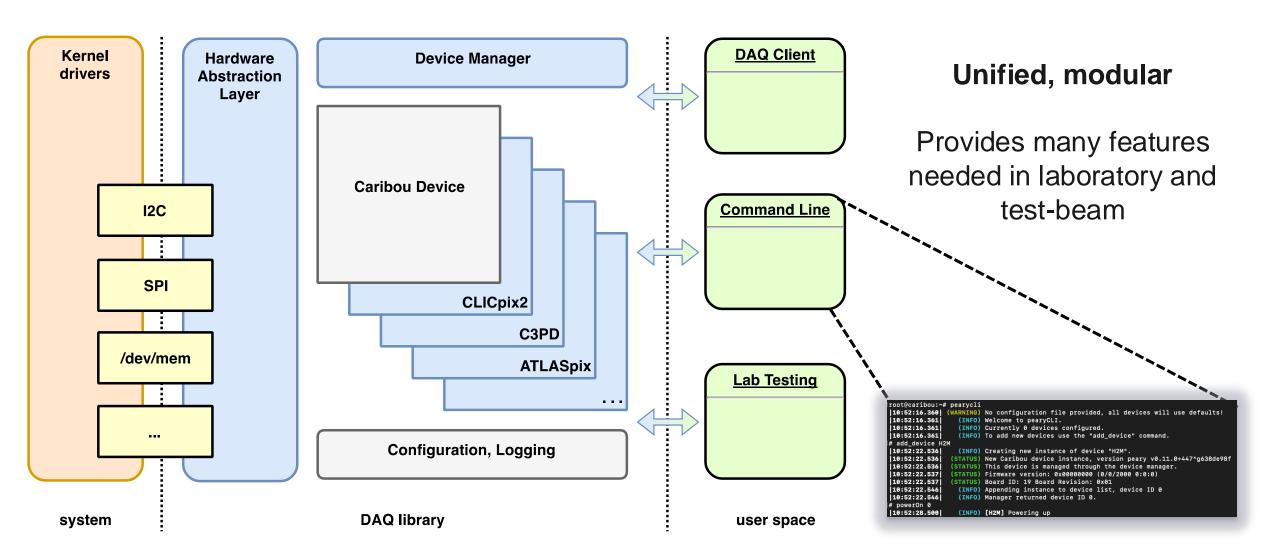


Integration pilot projects:

- > H2M: DESY, CERN
- ➤ MPW4: Sevilla University



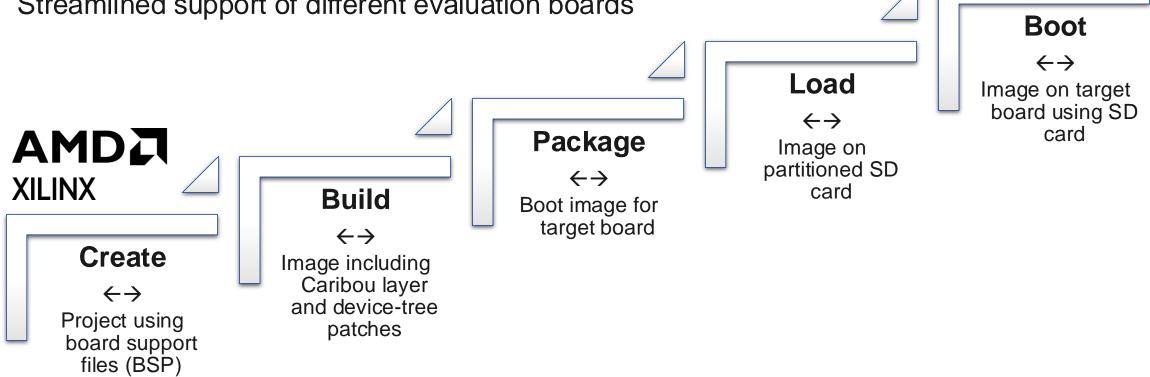
Caribou Peary software





Petalinux image builder

- Simplified workflow for boot image generation
- User-friendly image configuration
- Streamlined support of different evaluation boards





Device integration workflow

Design DUT chip board

Route signals to CaR connector according to pin mapping

Design DUT firmware core

Implement control and readout logic, and map to corresponding register interface

Integration and testing

Laboratory and test-beam characterization

Design DUT software class

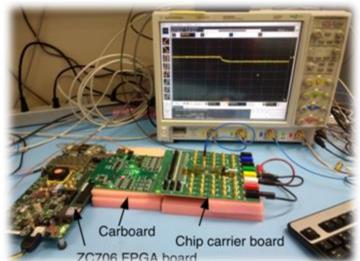
Define mapping of CaR board peripherals, firmware registers and implement interface functions



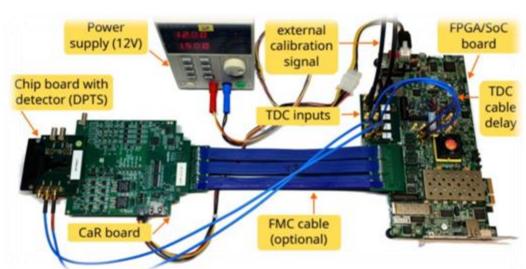
Application examples

- Support for various readout schemes
 - Digital interface via GTx or LVDS
 - Analogue waveforms (ADC or oscilloscope)
- Integration in beam telescope setups
 - Timepix3/SPIDR, Mimosa/EUDAQ, ALPIDE

FASTpix with oscilloscope readout



DPTS with TDC in FPGA readout



Telescope integration

CLICdp Timepix3 @ CERN





ALPIDE @ MAMI

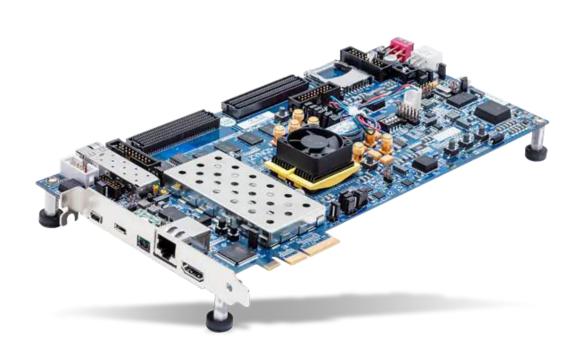




What's next?



Support of UltraScale+ MPSoC boards



Xilinx ZC706 evaluation board

Supported Not available anymore



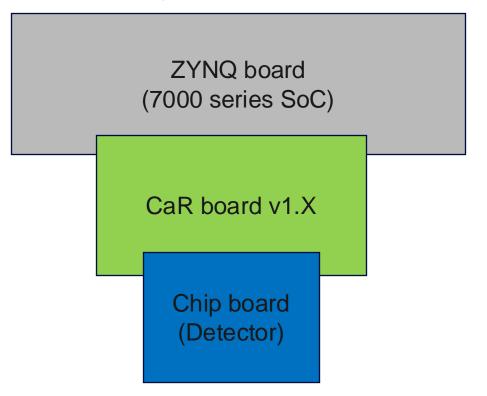
Xilinx ZCU102 evaluation board

Supported Intermediate step towards Caribou v2.0



Caribou v2.0

Caribou v1.X





Caribou v2.0

System-on-Module (Ultrascale+ MPSoC)

CaR board v2.0

Chip board (Detector)

Caribou v2.0

- Based on commercial System-on-Module (SoM)
 - Merge CaR board and ZYNQ board into a single board
 - Optimize system cost, increase flexibility and performance

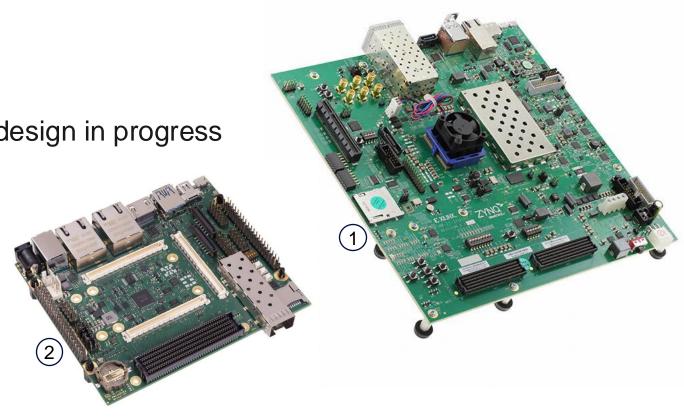


ZYNQ Ultrascale+ MPSoC

More resources and processing power

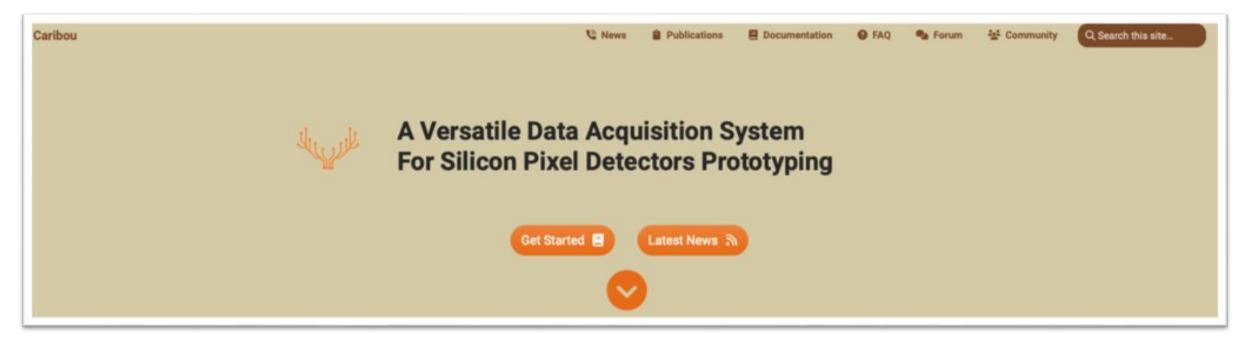
CaR board hardware specifications and design in progress

- Software/Firmware development phase
 - Support of compatible boards
 - 1) Xilinx <u>ZCU102</u>
 - 2) Mercury+ ST1





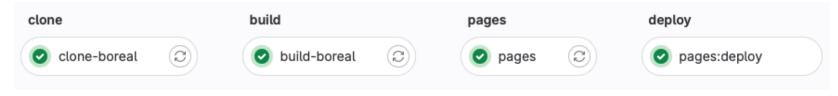
Documentation website



Project website

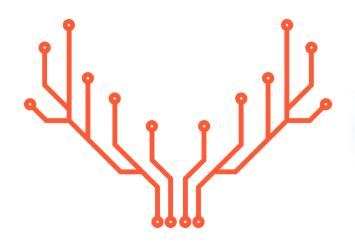
- Documentation
- Mattermost channel
- Publications
- Forum
- ...

Automatic documentation builds and website deployments





Summary





- Caribou is:
 - A versatile DAQ system for silicon pixel detectors
 - Open source, standalone
 - Proved excellent operation on many detector prototypes
 - Large community of users (including DRD3)
 - Ongoing upgrade phase with many improvements to come





Thank you

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Caribou system architecture

