

# Caribou: Overview of the system, recent developments and future plans

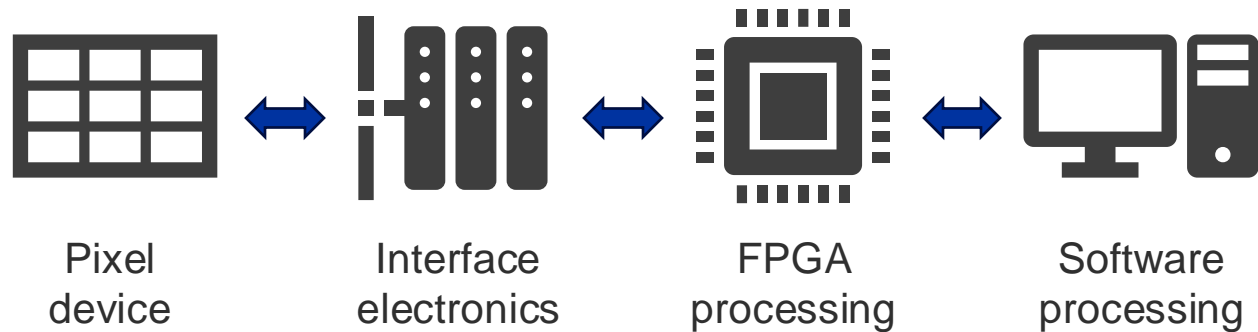
[Younes Otariid](#), Mathieu Benoit, Eric Buschmann, Hucheng Chen, Dominik Dannheim, Thomas Koffas, Ryan St Jean, Simon Spannagel, Shaochun Tang, Tomas Vanat

DRD3.1 Project Meeting – 29 November 2024

# System Overview

# A particular solution to a particular need

Most silicon pixel detectors share the same power, control and readout concepts  
(voltage/current supply, high speed data, communication protocols)

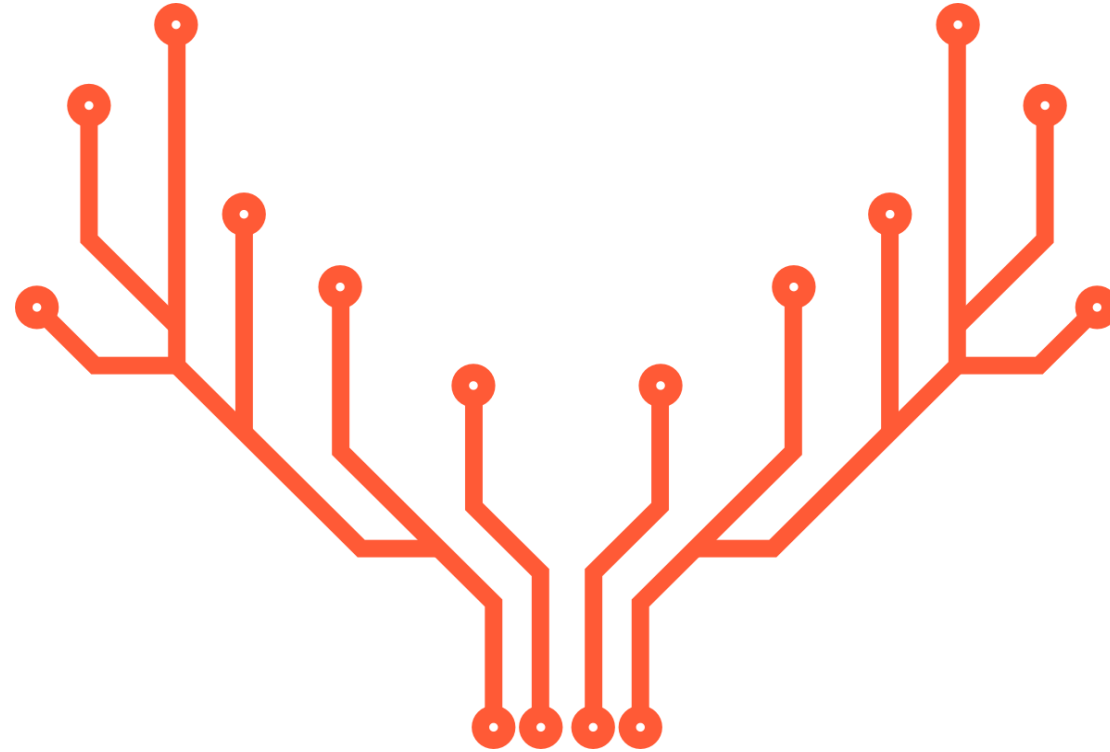


Every new prototype drives the development of a new DAQ system or modification of an existing one  
(time consuming, not very efficient)

## Why not a common versatile DAQ system ?

(Common hardware, firmware and software suit, keeping the focus of users on detector integration)

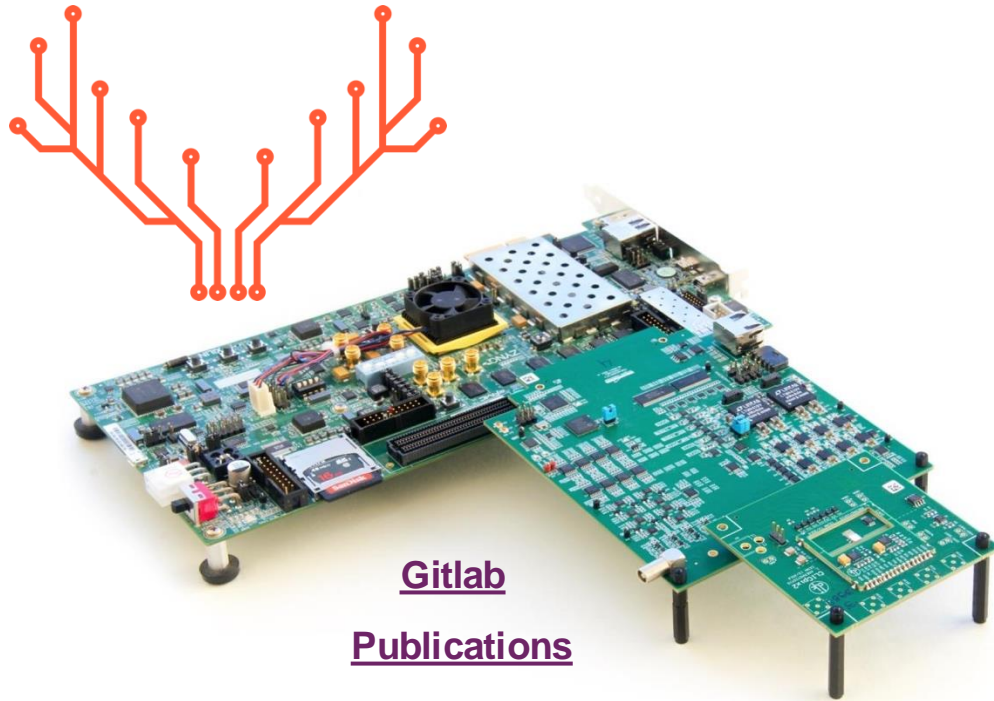
# A particular solution to a particular need



Caribou

# An open source common platform

Open source hardware, firmware and software for laboratory and beam tests

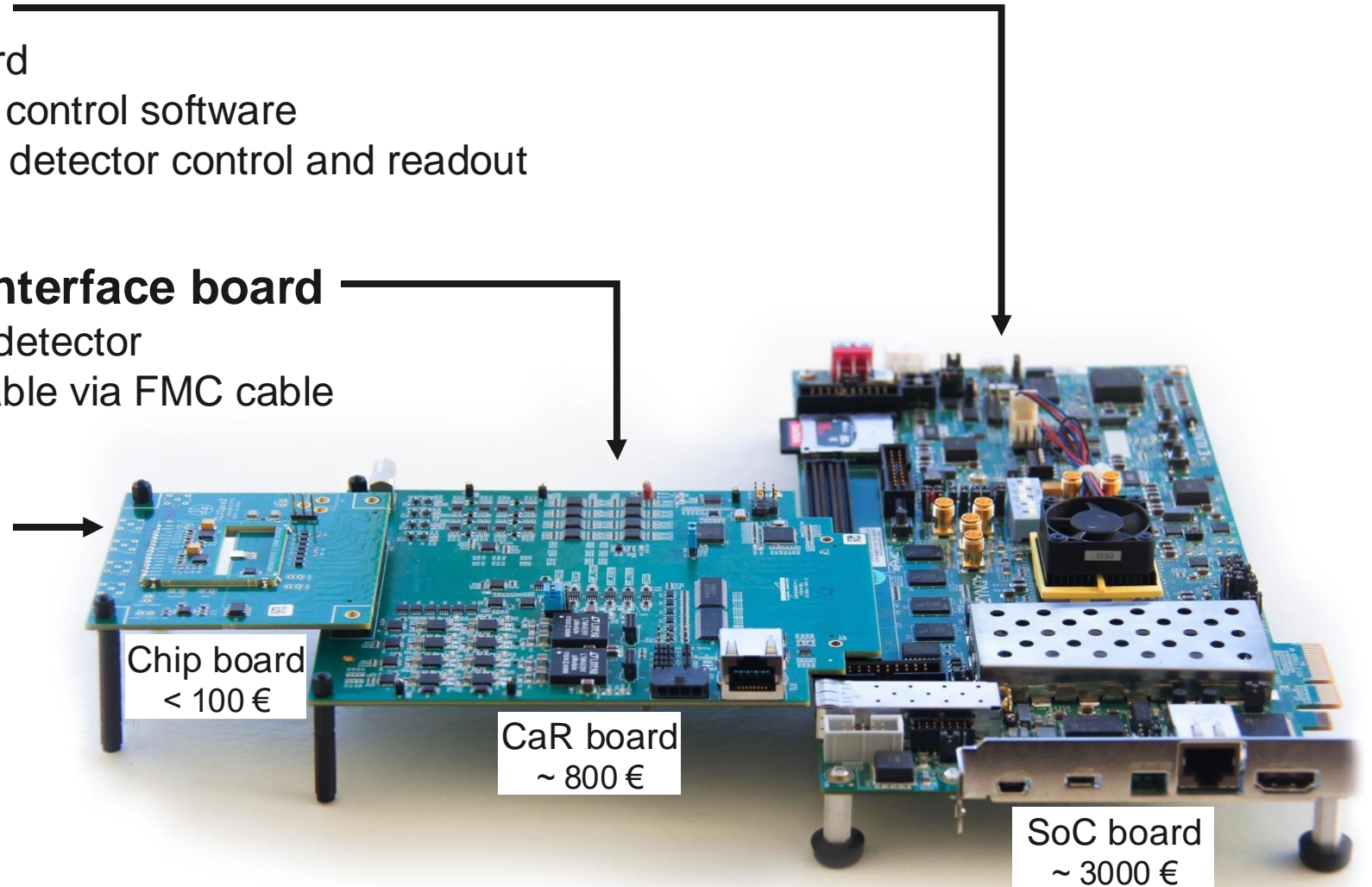


Developed by a collective effort of hardware, firmware and software developers



# A modular system architecture

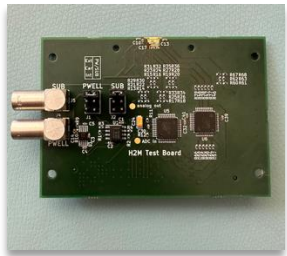
- **System-on-Chip (SoC) board**
  - ie: Xilinx ZC706 evaluation board
  - Embedded CPU runs DAQ and control software
  - FPGA runs custom firmware for detector control and readout
- **Control and Readout (CaR) interface board**
  - Physical interface from SoC to detector
  - CaR – SoC connection extendable via FMC cable
- **Detector (chip) carrier board**
  - Custom low-cost PCB
  - Designed by users



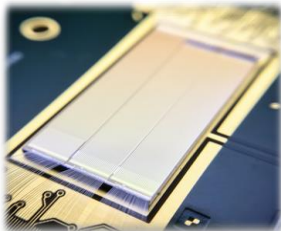
# A custom detector chip board

- **Detector-specific**
  - Physical hardware hosting the detector
  - Only provide passives and detector-specific components
- **Multiple detectors already integrated and tested:**

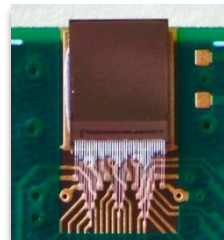
H2M



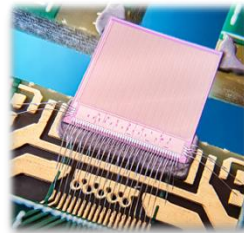
ATLASpix



CLICpix2



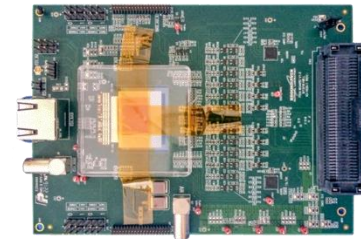
CLICTD



FASTPIX



H35Demo/FEI4



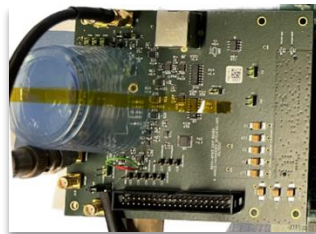
RD50-MPW1



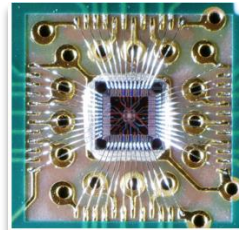
RD50-MPW2



RD50-MPW3



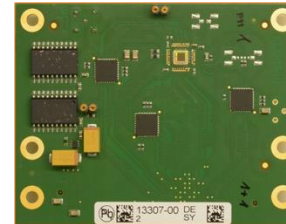
APTS



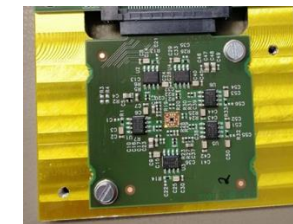
DPTS



dSiPM



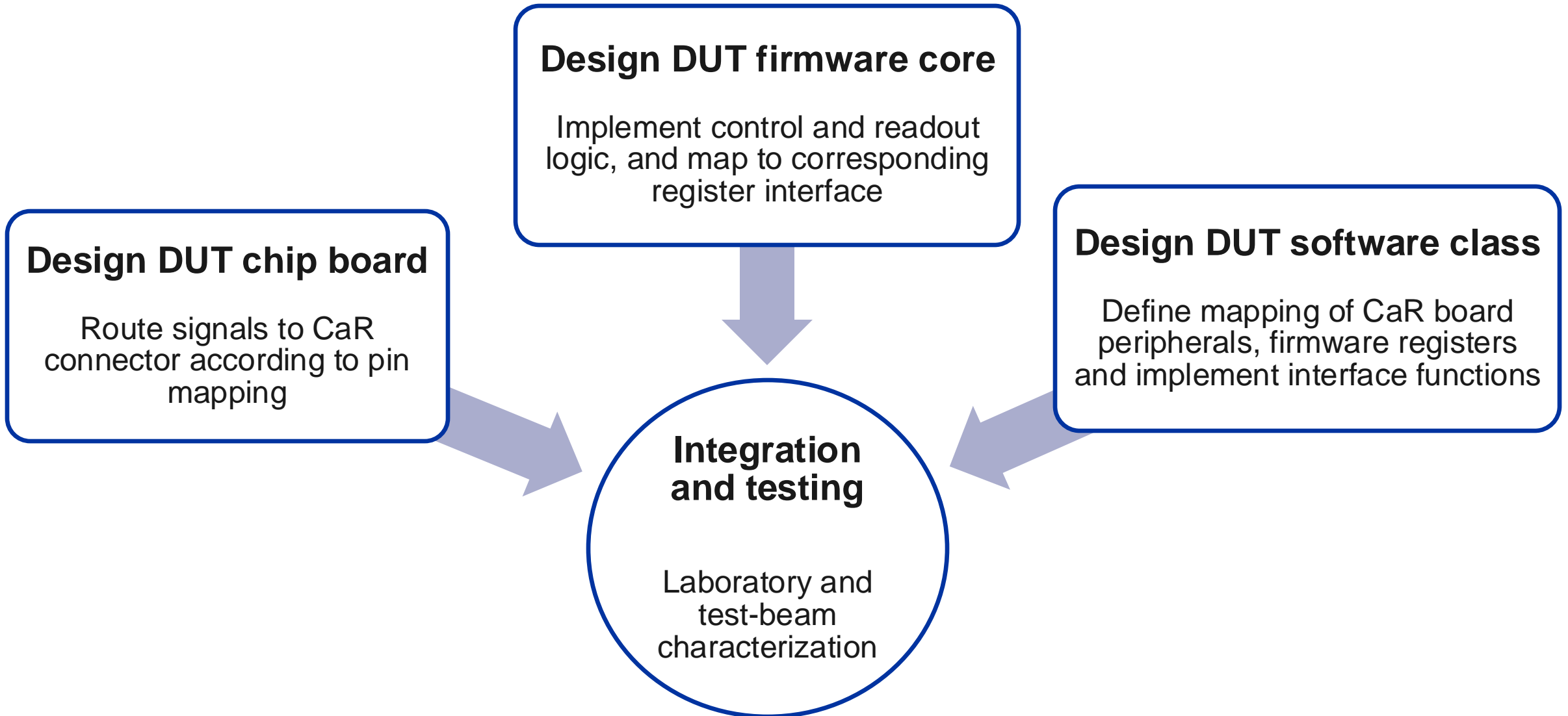
MLR1



CoRDIA



# Device integration workflow





# Application examples

- Support for various readout schemes
  - Digital interface via GTx or LVDS
  - Analogue waveforms (ADC or oscilloscope)
- Integration in beam telescope setups
  - Timepix3/SPIDR, Mimosas/EUDAQ, ALPIDE

MIMOSA @ DESY

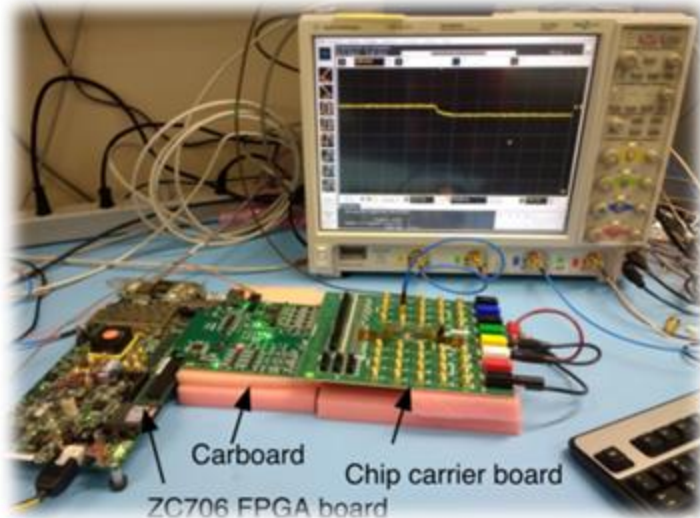


Telescope integration

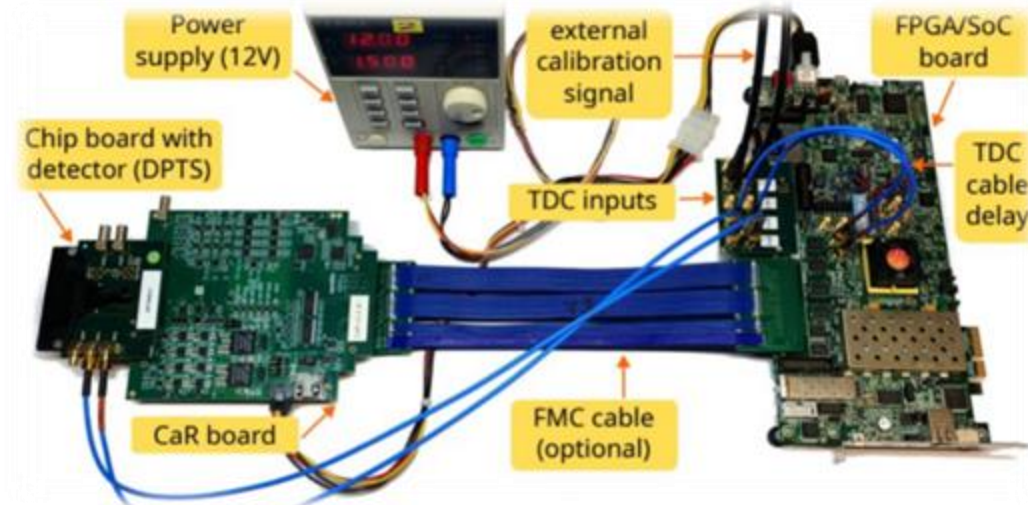
CLICdp Timepix3 @ CERN



FASTpix with oscilloscope readout



DPTS with TDC in FPGA readout



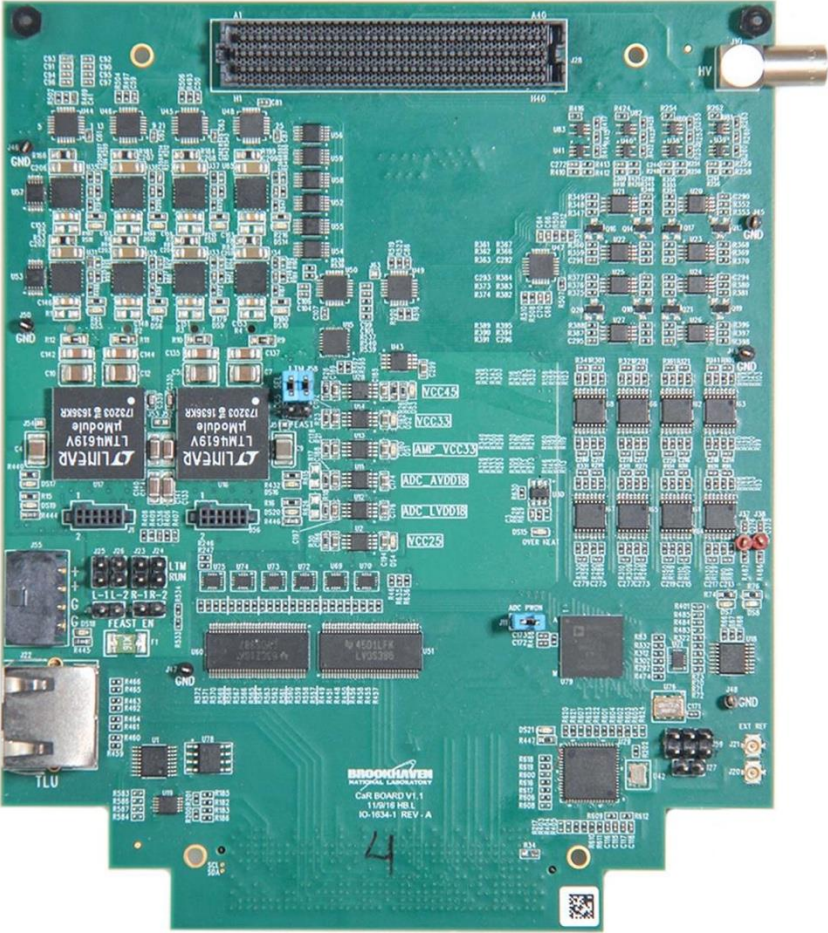
ALPIDE @ MAMI



# System Status

# CaR board - Overview

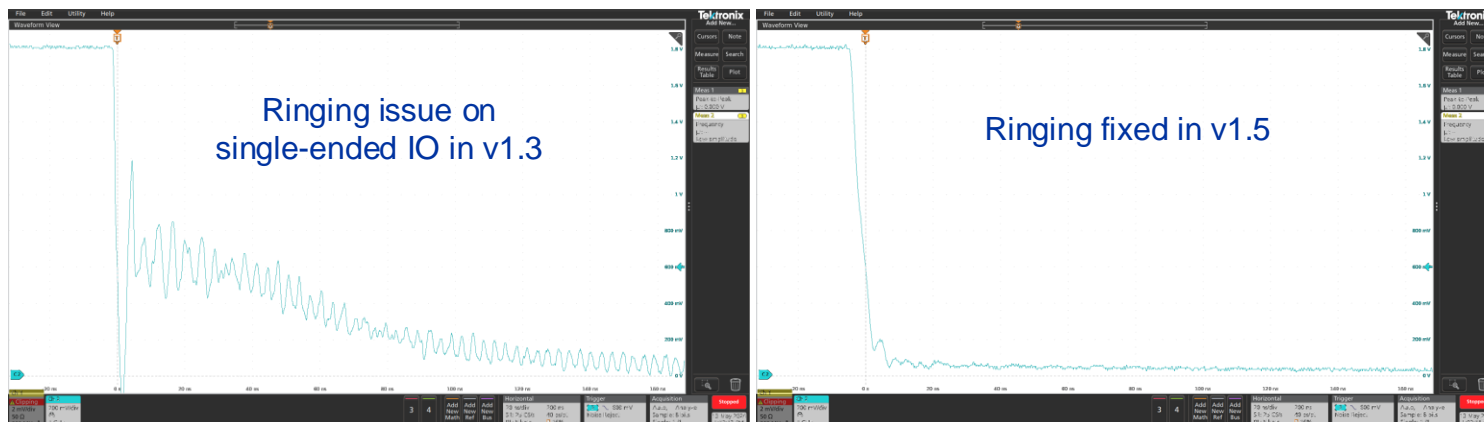
Feature	Description
Adjustable Power Supplies	8 units, 0.8 – 3.6 V, 3 A
Adjustable Voltage References	32 units, 0 – 4 V
Adjustable Current References	8 units, 0 – 1 mA
Voltage Inputs to Slow ADC	8 channels, 50 kSPS, 12-bit, 0 – 4 V
Analog Inputs to Fast ADC	16 channels, 65 MSPS, 14-bit, 0 – 1 V
Programmable Injection Pulsers	4 units
Full-Duplex High-Speed GTx Links	8 links, <12 Gbps
LVDS Links	17 bidirectional links
Input/Output Links	10 output links, 14 input links, 0.8 – 3.6 V
Programmable Clock Generator	Included
External TLU Clock Reference	Included
External High-Voltage (HV) Input	Included
FEAST Module Compatibility	Supported
FMC Interface to FPGA	Included
SEARAY Interface to Detector Chip	320-pin connector



More than 50 CaR boards to 14 institutes

# CaR board v1.5 release

- Response to high CaR board demands
- Respin of CaR board v1.4
  - Replacement of obsolete components
  - Small improvements and bug fixes
- Production and distribution of 31 boards
  - RD50 + DRD3 common funds (pending validation)
  - Production granted to Safiral, Czechia
  - Distributed in August 2024 to 10 institutes



# CaR board v1.5 release

- Response to high CaR board demands

- Respin of  
• Repla  
• Small

- Producti  
• RD50  
• Produ  
• Distri

**Currently collecting requests for another combined purchase order  
Please contact us in case you would like to take part**

## Contacts:

[caribou-developers@cern.ch](mailto:caribou-developers@cern.ch)

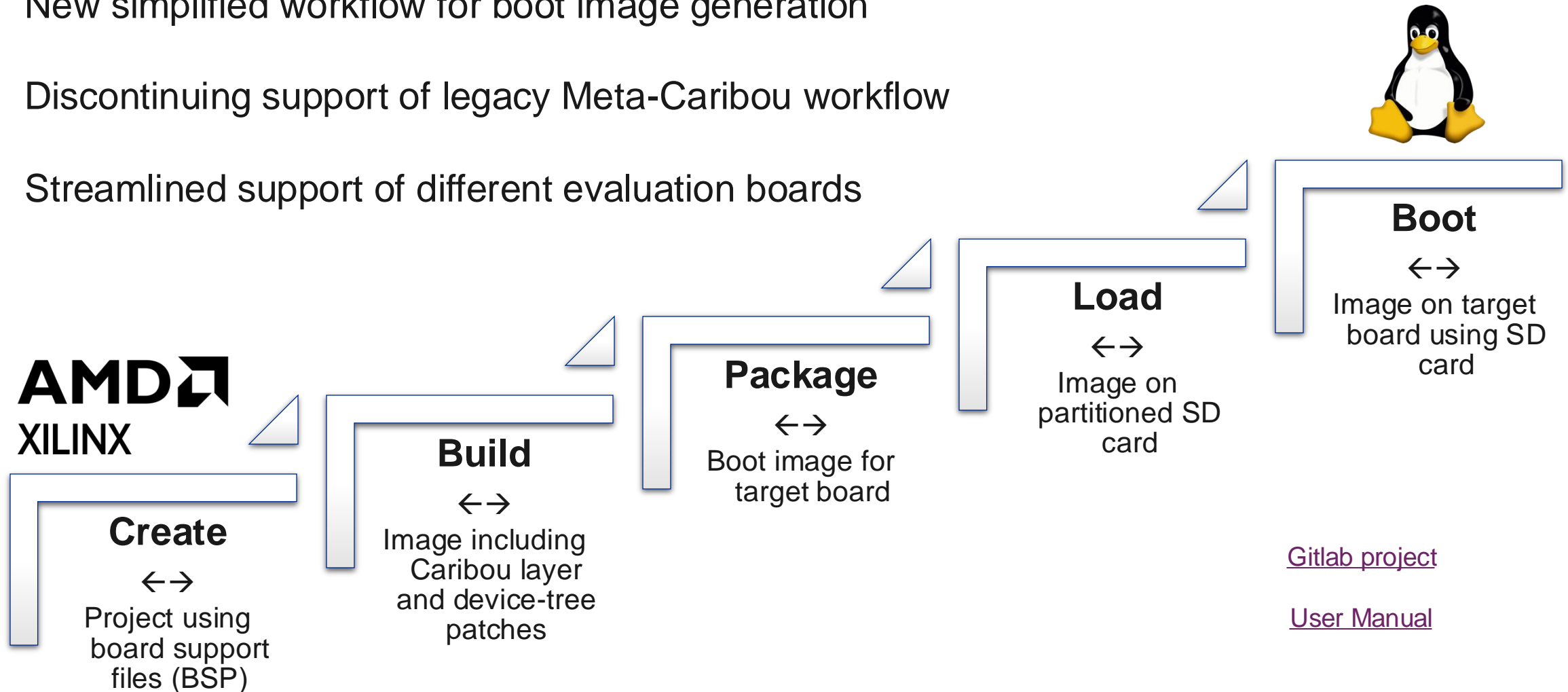
or

[dominik.dannheim@cern.ch](mailto:dominik.dannheim@cern.ch)

[younes.otarid@cern.ch](mailto:younes.otarid@cern.ch)

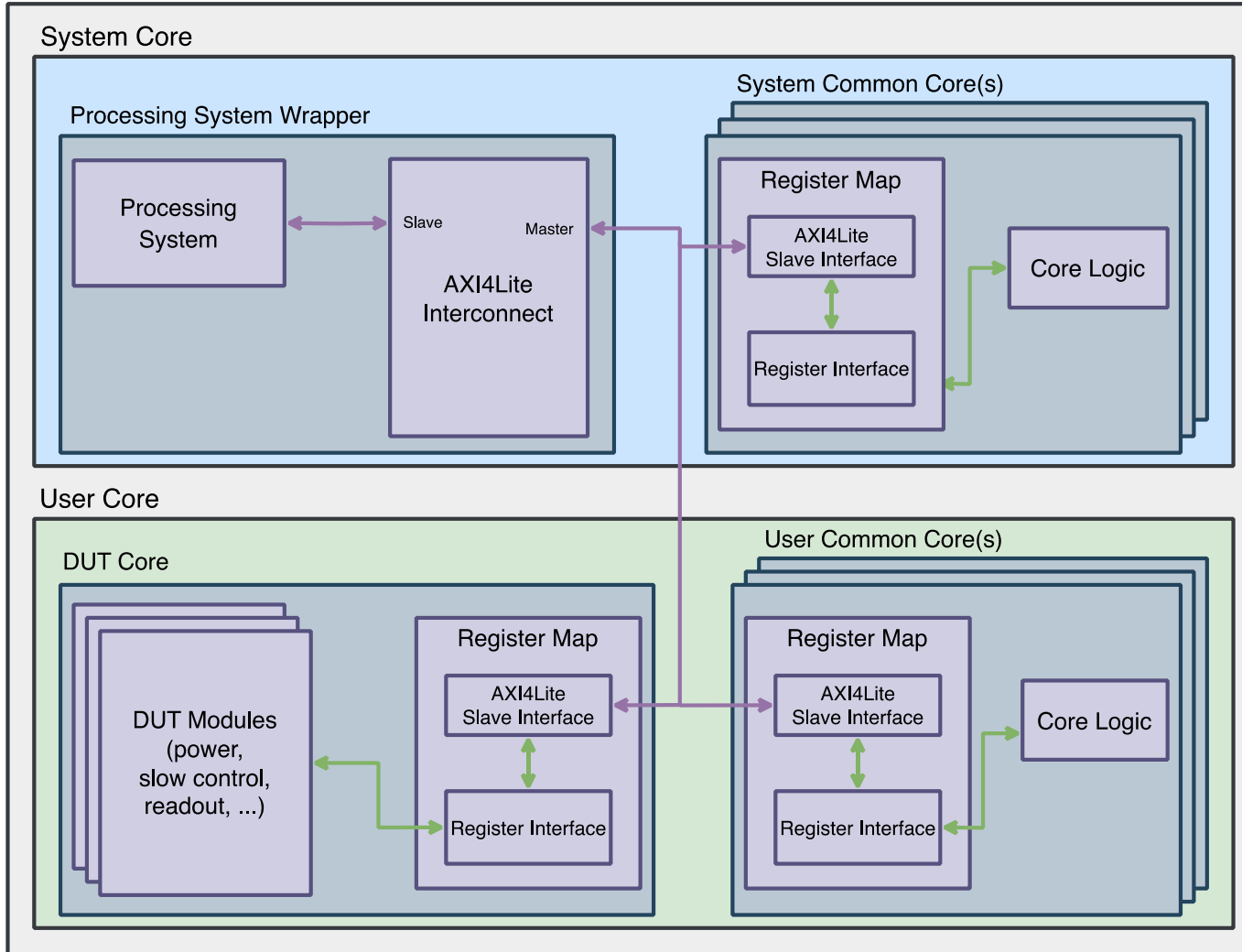
# Peta-Caribou: Petalinux OS image builder

- New simplified workflow for boot image generation
- Discontinuing support of legacy Meta-Caribou workflow
- Streamlined support of different evaluation boards

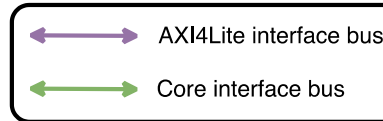


# Boreal: Unified FPGA firmware

Top Module



Legend

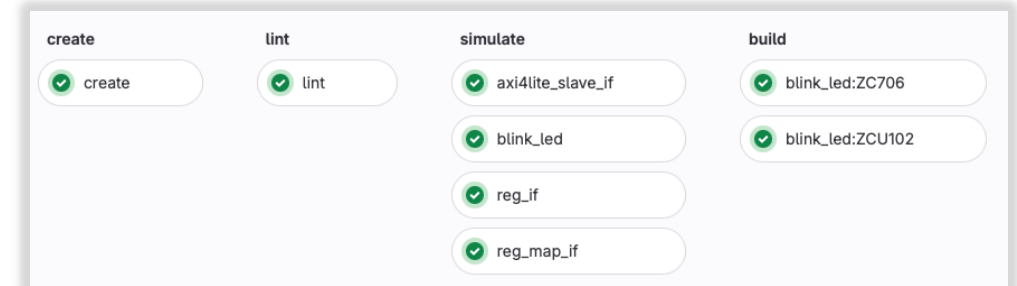


[Gitlab project](#)

User Manual preparation ongoing

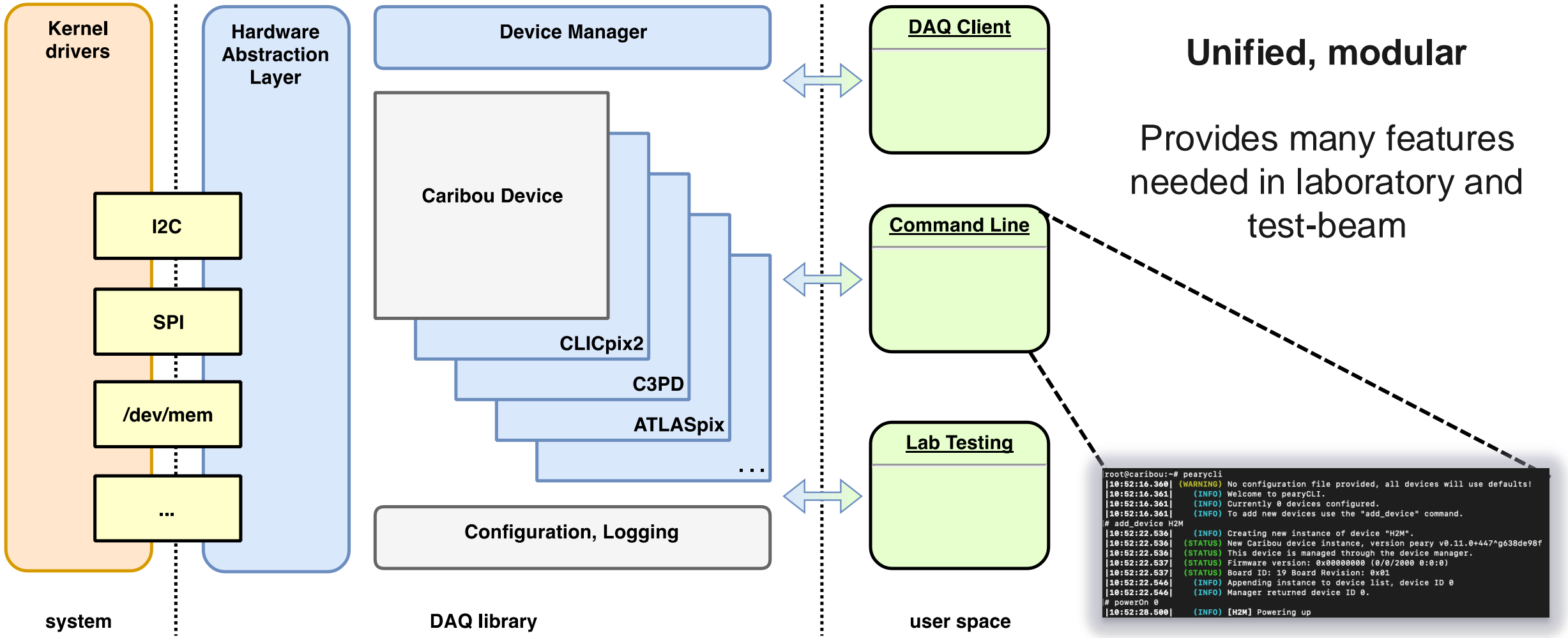
**Unified, modular and configurable**  
Support of multiple boards + devices

**Streamlined CI/CD workflow**  
Simulation, building and bitfile release



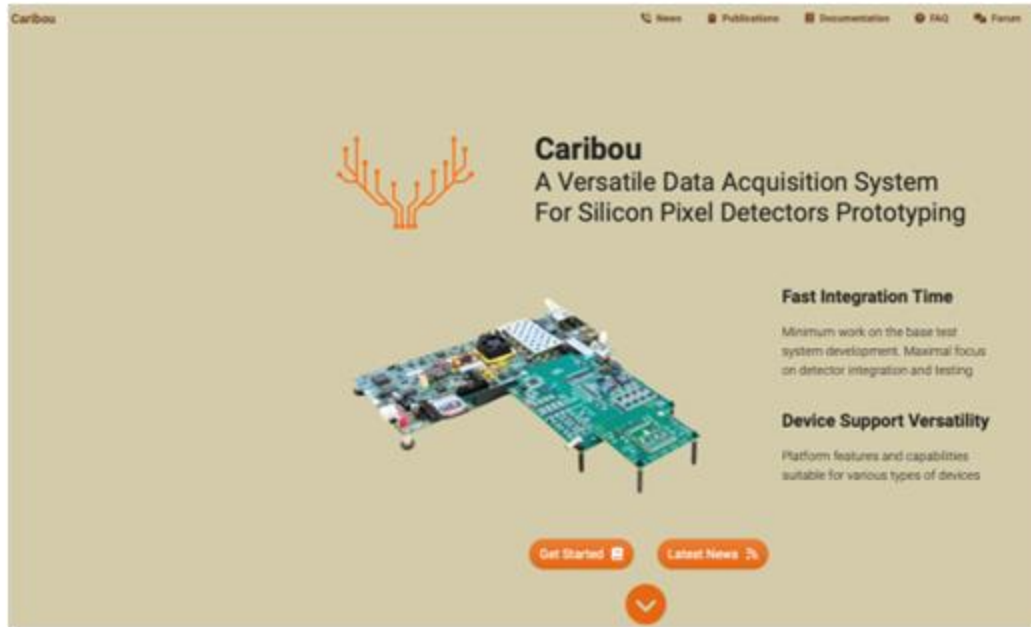
**Pilot project**  
H2M : DESY, CERN

# Peary: Software Framework





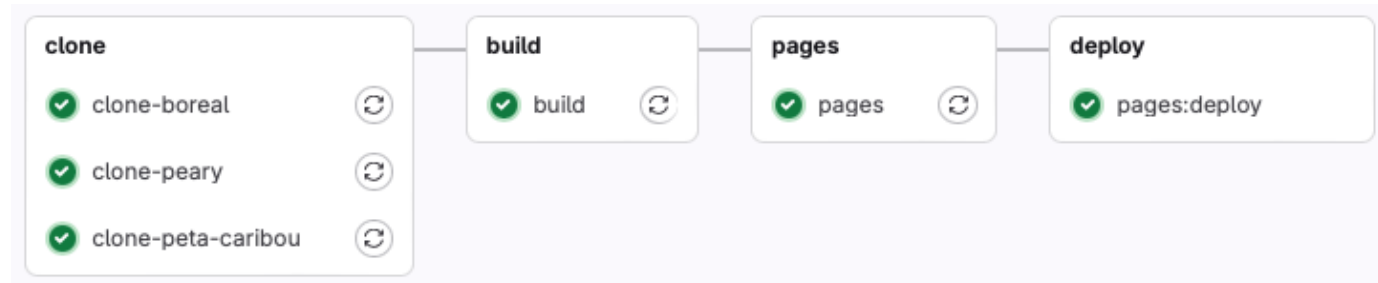
# Project website and documentation



## Project website

- Documentation
- Mattermost channel
- Publications
- Forum
- ...

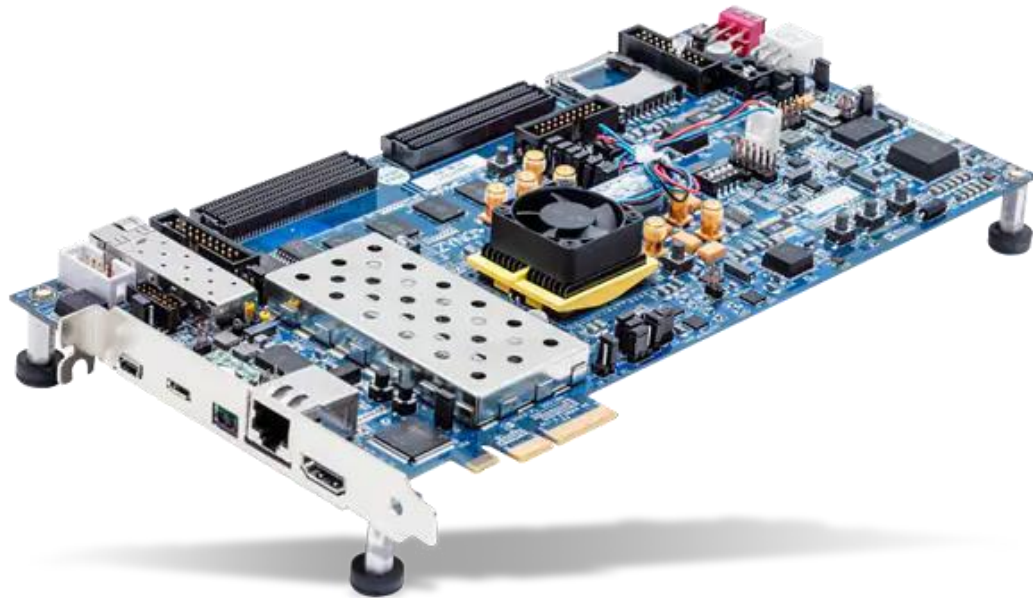
## Automatic documentation builds and website deployments



[Gitlab project](#)

# Future Plans

# Support of UltraScale+ MPSoC boards



Xilinx ZC706 evaluation board

**Supported**  
**Not available anymore**



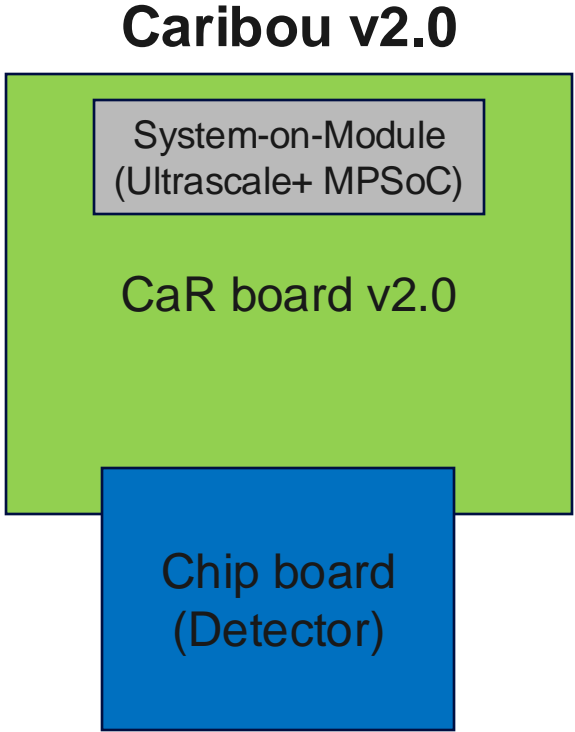
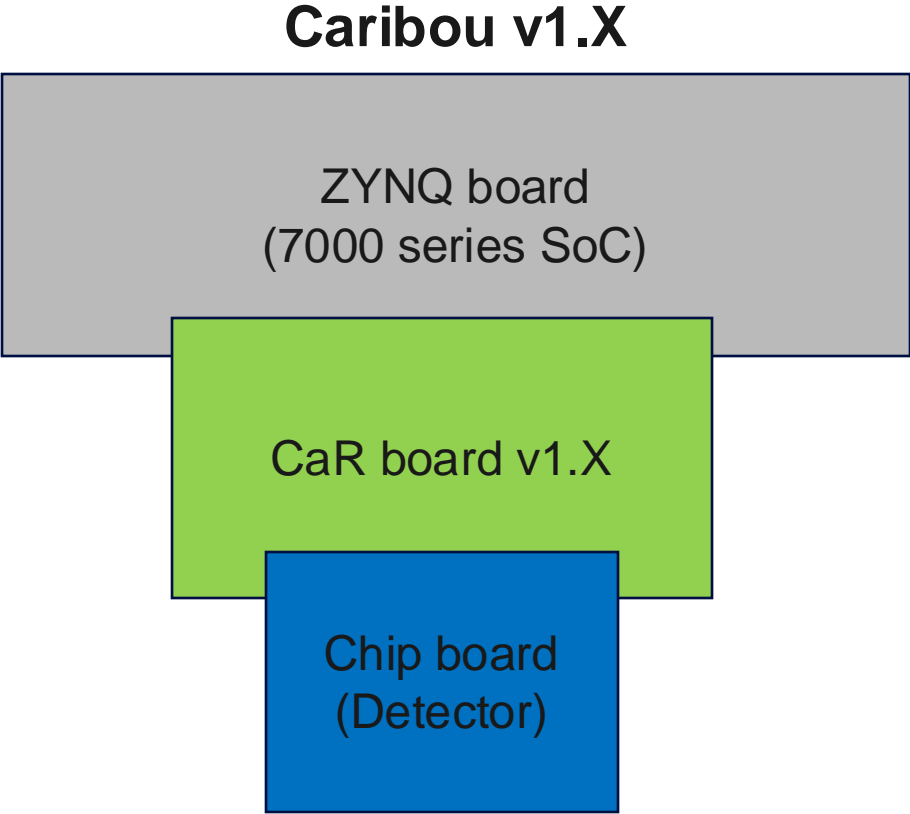
Xilinx ZCU102  
evaluation board

Enclustra  
Mercury+ ST1



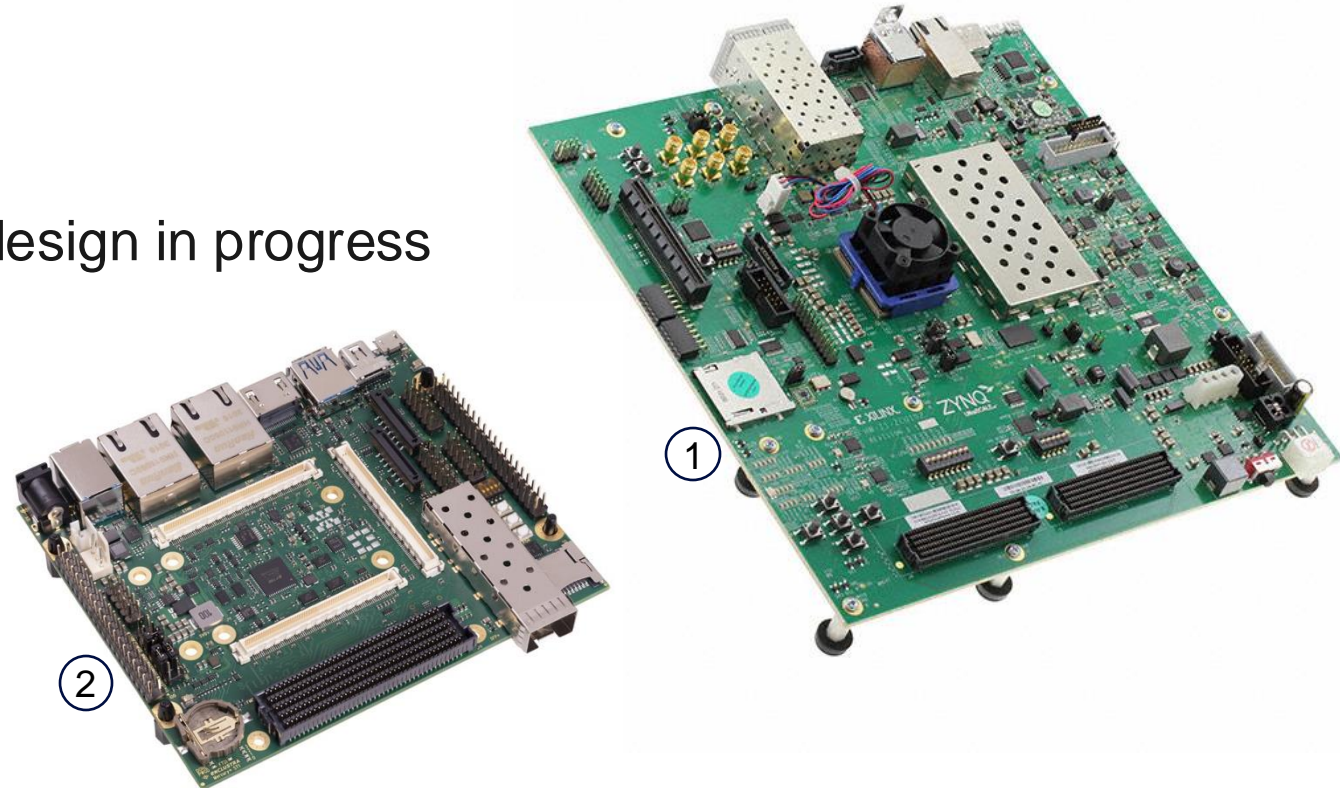
**Ongoing work to support**  
**Intermediate step towards Caribou v2.0**

# Caribou v2.0



# Caribou v2.0

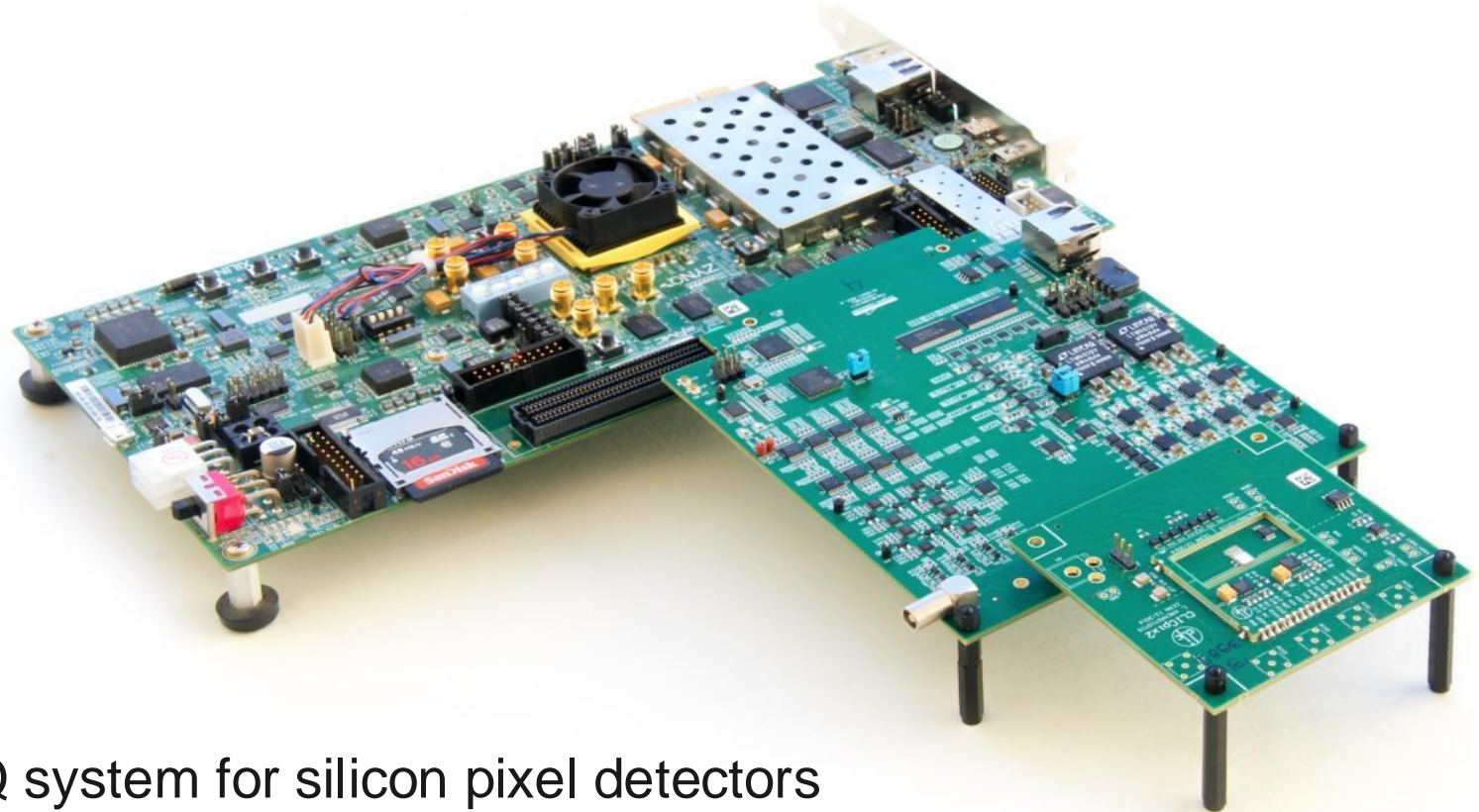
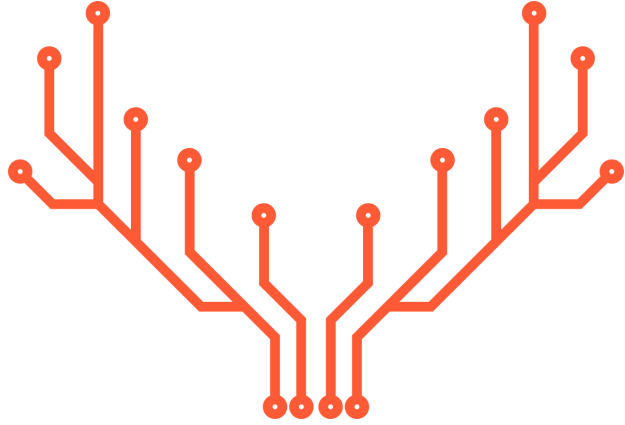
- Based on commercial **System-on-Module (SoM)**
  - Merge CaR board and ZYNQ board into a single board
  - Optimize system cost, increase flexibility and performance
- Mercury+ XU1 System-on-Chip
  - ZYNQ Ultrascale+ MPSoC
  - More resources and processing power
- CaR board hardware specifications and design in progress
- Software/Firmware development phase
  - Using UltraScale+ MPSoC boards
    - 1) Xilinx ZCU102
    - 2) Mercury+ ST1



# Caribou v2.0 Test Board

- Next step towards Caribou 2
  - Smaller test board without SoM and fewer channels
  - Controlled via USB
- Goals:
  - Test and characterize analog circuits and power supplies
  - Evaluate different design options
- Improvements include:
  - Increased range for power supplies and current sources
  - Negative supply voltages
  - Improved overcurrent protection
- Schematic design is being reviewed and prepared for layout
- Will be scaled up to full design with all channels and SoM after testing

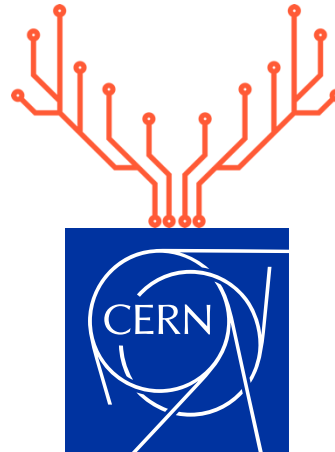
# Summary



- Caribou is:
  - A versatile DAQ system for silicon pixel detectors
  - Open source, standalone
  - Proved excellent operation on many detector prototypes
  - Large community of users (including DRD3)
  - Ongoing upgrade phase with many improvements to come



# Thank you



## Contact

CERN  
Younes Otarid  
EP R&D  
[younes.otarid@cern.ch](mailto:younes.otarid@cern.ch)

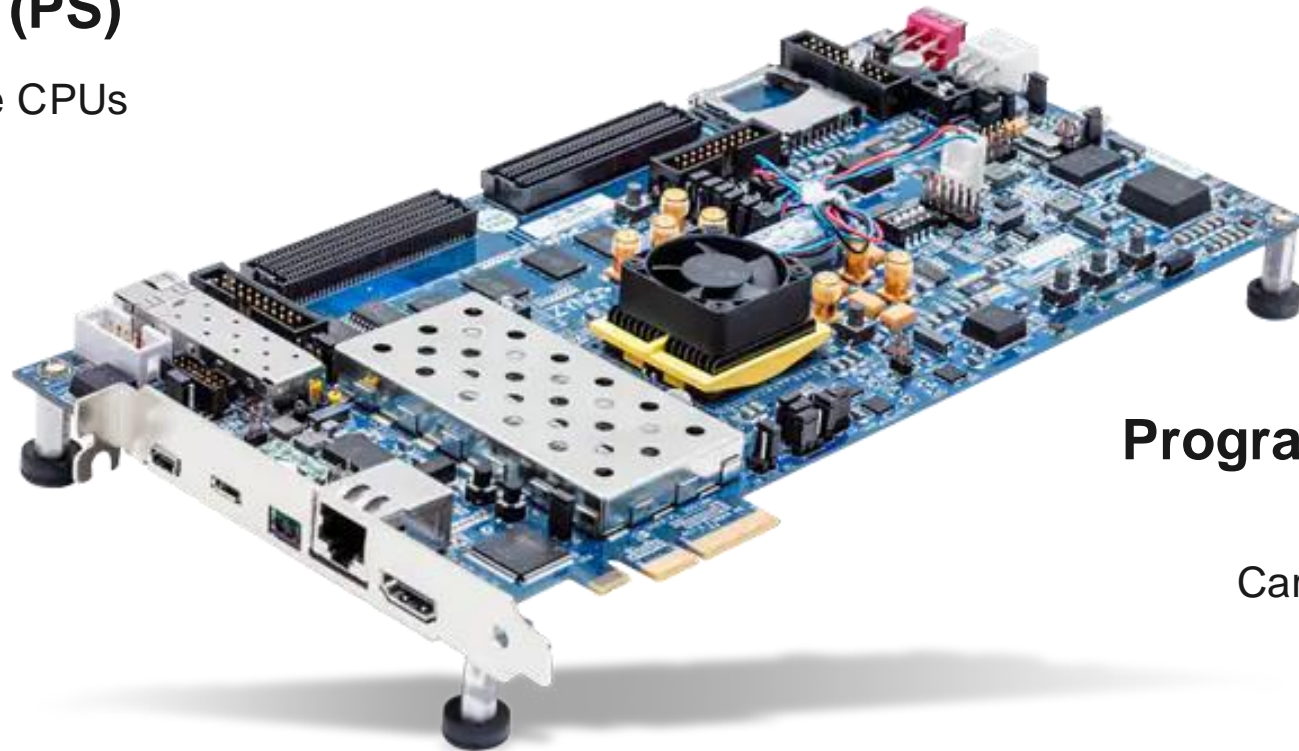
[home.cern](http://home.cern)



# A commercial System-on-Chip board

## Processing System (PS)

2 x ARM Cortex-A9 MPCore CPUs  
Petalinux image  
Caribou software



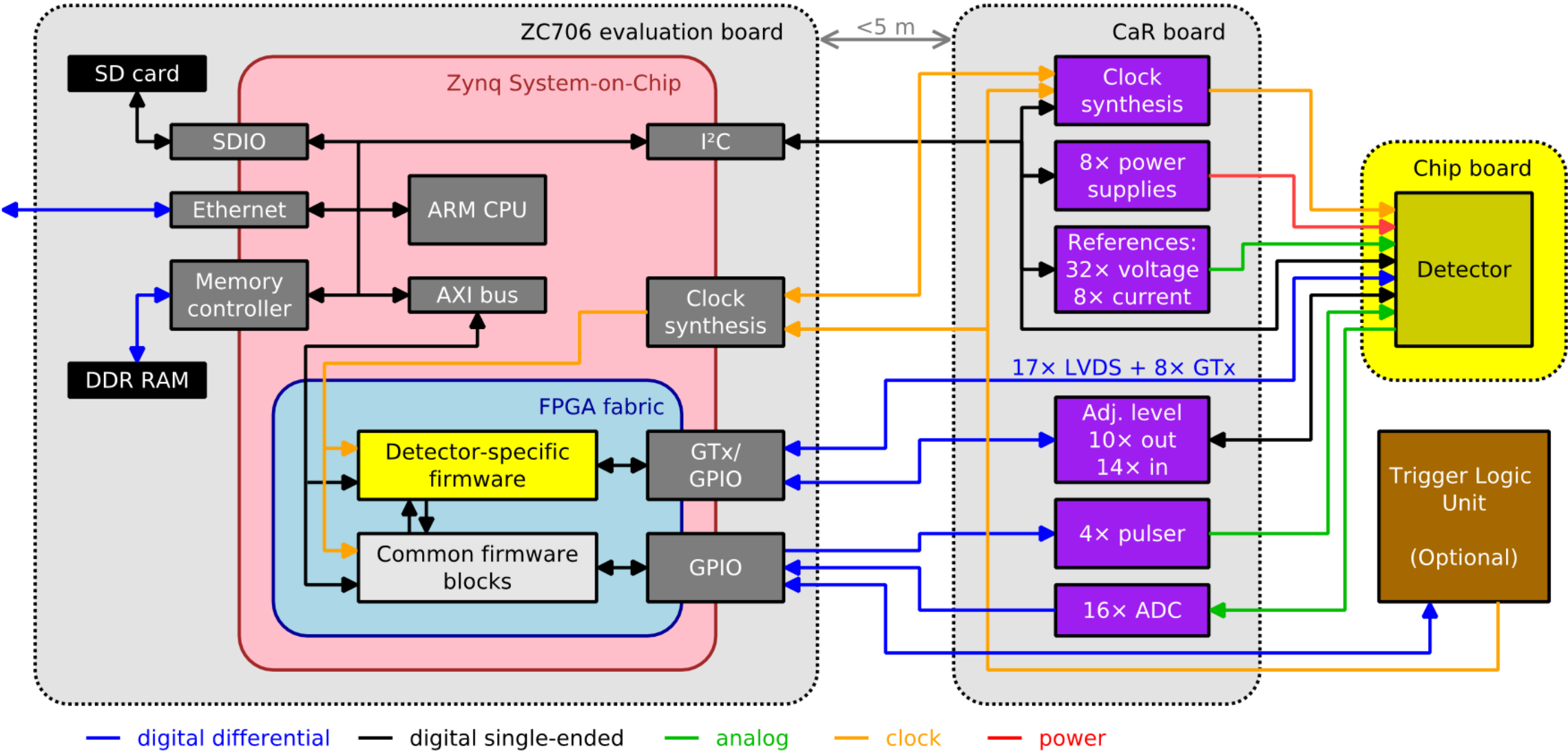
## Programmable Logic (PL)

Kintex-7 FPGA  
Caribou FPGA firmware



Xilinx ZC706 evaluation board

# Caribou system architecture



# Peta-Caribou: Petalinux OS image builder

